



News Release

Waltham, MA,

CARBON BREAKS SW VALIDATION BARRIER

*Replay™ Solves Software Validation Bottleneck for Iterations
through Previously Validated Code*

WALTHAM, MA – June 22, 2006 - Carbon Design Systems — a leader in virtual system prototyping—announced today that it will introduce major new functionality for its SOC-VSP product line at this year’s Design Automation Conference. ESL simulation environments typically contain models at different levels of abstraction, accuracy, and performance including: behavioral, instruction-level, transaction-level, cycle-accurate, and bus transactors that maintain state information. Developers validating software on a system model must iterate through all their previously validated code when adding new functionality or debugging problems that may have occurred hours into a simulation. While this isn’t a performance issue if all the simulation models are homogeneous at the highest levels of abstraction, it is a throughput issue as accuracy is introduced to the system model through IP integration and RTL implementation. Carbon’s Replay removes this performance barrier to incorporating RTL into a heterogeneous modeling environment by enabling rapid software iterations through validated code and interactive software debug, while maintaining the underlying cycle-accuracy.

“By eliminating the need to rerun the ‘Carbonized’ hardware model for each software iteration, simulation throughput can be boosted by one to two orders of magnitude,” said Alan Swahn, Vice President of Marketing at Carbon Design Systems. “Our Replay technology enables RTL to be included in an ESL environment, while maintaining performance for software developers.”

About Replay

Software developers commonly iterate through previously validated code many times in the design and validation process. The underlying system model of the hardware components is usually high-performance, but not cycle-accurate. Unfortunately, this limits the degree to which software drivers and embedded firmware can be validated before a physical prototype is available. This delays software development starting in earnest until late in the design cycle. Replay is a novel idea to break this performance-accuracy logjam.

‘Carbonized’ cycle-accurate RTL models can record incoming bus traffic and response for an initial simulation and save the model state information at specified intervals. During the next software execution iteration, the Carbonized model is stimulated from other abstract components in the system and replays its saved response at very high speed until the last valid checkpoint, at which time the Carbonized model restores its state and simulates normally from that point

forward. Replay mode will detect any inputs that don't match in sequence or value and automatically rollback to the previous checkpoint to ensure correct operation. Replay performance enables interactive software debugging.

About Carbon

Carbon is delivering a high-performance virtual system prototyping solution that enables an ASIC or SoC prototype to be rapidly assembled and functionally validated on an engineer's desktop months before silicon. Carbon's new software approach allows multiple levels of abstraction to be validated together including processors, peripherals, C, SystemC, Verilog, VHDL, IP cores, and transaction-level models. The key to VSP is silicon accuracy and performance -- the ability to execute billions of cycles and boot embedded operating systems, all with desktop software. Problems can be found and resolved during the design cycle -- rather than waiting for idealized behavioral models to be developed or first silicon to be delivered.

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