



News Release

Waltham, MA,

Carbon's VSP(TM) Lineup Adds PCI, PCI-X, USB2.0, SDRAM Bus Protocols

New Transactors Enable Fast Transaction-Level Simulation

WALTHAM, MA - December 20, 2005 - Carbon Design Systems -- a leader in virtual system prototyping -- announced today that it has added PCI, PCI-X, USB 2.0 Host, and DDR SDRAM bus protocol support to its VSP product line. These bus functional models (transactors) provide a communication layer from abstract functions, such as reads and writes, to pin-level devices listening/responding on a bus. The combination of a transactor and 'Carbonized' RTL (virtual hardware model) creates a high-performance transaction-level model (TLM) that is easy to integrate into diverse heterogeneous modeling environments that may contain instruction set simulators, idealized behavioral models, and cycle-accurate models.

"This is just the start of Carbon's transactor library for standard bus protocols," said Alan Swahn, Vice President of Marketing at Carbon Design Systems. "Transactors are a requirement for mixing levels of abstraction in ESL environments and are a natural addition to drive simulation performance and ease-of-use with our products."

ESL Transactors

Transactors translate a high-level abstracted view of protocol operations -- reads, writes, burst transfers, idle, busy, reset, interrupts -- into a proper sequence of signal transitions for each operation over a definitive number of clock cycles. A bus transaction describes the data being exchanged between devices, whereas the signal or pin-level establishes how the data is exchanged during the transaction. A bus transaction is typically modeled as a function call, with the data being exchanged as parameters to the call. Particular bus behavior may be configurable, depending on the transactor, including address and data widths, burst length, and endianness.

Pricing and Availability

Carbon's PCI, PCI-X, USB2.0 Host, and DDR SDRAM transactors will be shipping December 30, 2005 as options to Carbon's VSP product. Pricing per seat is based on an annual subscription volume model.

About Carbon

Carbon is delivering a high-performance virtual system prototyping solution that enables an ASIC or SoC prototype to be rapidly assembled and functionally validated on an engineer's desktop months before silicon. Carbon's new software approach allows multiple levels of abstraction to be validated together including processors, peripherals, C, SystemC, Verilog, VHDL, IP cores, and transaction-level models. The key to VSP is silicon accuracy and performance -- the ability to execute billions of cycles and boot embedded operating systems, all with desktop software. Problems can be found and resolved during the design cycle -- rather than waiting for idealized behavioral models to be developed or first silicon to be delivered.

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