News Release

Waltham, MA,

Carbon Joins 0-In's Check-In Program

Expands Hardware Regression Reach

WALTHAM, MA, July 29, 2004, Carbon Design Systems-a fast moving EDA company that reduces time-to-profit for chip companies by improving hardware regression performance and enabling pre-silicon system validation-announced today that it has joined the 0-In Design Automation's Check-In Partner Program, signaling Carbon's growing presence in RTL verification flows.

Design size and complexity have skyrocketed, but existing eighties-era simulators have failed to keep pace with the growing verification challenge. The assertion synthesis capability of 0-In's Archer Verification System coupled with Carbon's high-performance DesignPlayer engine, offers a state-of-the-art solution that provides superior design bug identification, without sacrificing runtime performance.

"Our joint customers want to find bugs in their designs as quickly, cheaply and thoroughly as possible," remarked Steve White, President and CEO of 0-In. "Combining Carbon's high-performance DesignPlayer with the advanced assertion synthesis capability of the 0-In Archer Verification System makes that goal achievable."

"Many design teams are in the unenviable position of trying to solve today's daunting verification problem with yesterday's tools," commented Steve Butler, President and CEO of Carbon. "We're finding that many customers who choose DesignPlayer for a 10 to 50x improvement over their existing simulators, are also using 0-In's assertion synthesis to uncover bugs. Providing these customers with a turn-key solution is a necessity."

About SPEEDCompiler and DesignPlayer

Carbon's SPEEDCompiler software reads synthesizable Verilog, VHDL, or mixed language and generates a high-performance engine-DesignPlayer. DesignPlayer can represent one or more chips and multiple engines can represent a system that encompasses hundreds of millions of gates. DesignPlayer is a soft-model that is accurate to the hardware-cycle and register accurate. Unlike behavioral models or C models generated from an ideal specification, DesignPlayer behaves exactly like the hardware with all its errata.

About 0-In

0-In Design Automation, Inc. (pronounced "zero-in") develops and supports functional verification products that help verify multi-million gate application-specific integrated circuit (ASIC) and system-on-chip (SoC) designs. The company delivers a comprehensive assertion-based verification (ABV) solution built on industry standards that provides value throughout the design and verification cycle-from the block level to the chip and system levels. Twelve of the fifteen largest electronics companies have adopted 0-In tools and methodologies in their integrated circuit (IC) design verification flows. 0-In was founded in 1996 and is based in San Jose, CA. For more information, see www.0-in.com.

About Carbon Design Systems
Carbon is delivering software products that enable high-performance pre-silicon chip and system validation. Carbon's single engine solution-DesignPlayer-can be used for hardware, software, and customer design validation. The DesignPlayer engine boosts hardware regression performance and validates drivers, diagnostics, and firmware up to 50X faster with cycle and register accuracy. A low-cost executable or linkable model can be deployed across the enterprise and to customers without the encumbrances of a slow simulator.
Carbon's new approach shortens schedules and accelerates time-to-profit by enabling validation to occur in parallel with hardware development. Product schedules can be cut significantly, with validation starting as early as the first stable RTL. Problems are found and resolved before fabrication-rather than waiting for custom models to be built or silicon to be delivered..

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