



News Release

Waltham, MA,

Carbon's DesignPlayer™ Engine Executes in CoWare's SystemC Simulator

High-Performance RTL Engine Linked into SystemC

WALTHAM, MA, June 28, 2004, Carbon Design Systems-a fast moving EDA company that reduces time-to-profit for chip companies by improving hardware regression performance and enabling pre-silicon system validation-announced today that it has integrated Carbon's DesignPlayer engine into CoWare's ConvergenSC SystemC simulator and joined CoWare's CoTeam partnership program.

"This landmark integration allows RTL to be executed in CoWare's SystemC simulator," emphasized Steve Butler, president and CEO of Carbon. "Our joint customers can now use a SystemC simulator with the freedom to swap between an architectural model and the RTL model of a design while maintaining the performance required for software validation."

"Carbon's DesignPlayer integration enables mutual customers to incorporate legacy IP into high speed SystemC simulations using ConvergenSC," said Mark Milligan, VP of Marketing at CoWare. "This complements our SystemC ConvergenSC Model Library containing 3rd party IP, by giving customers the ability to use DesignPlayer to generate fast software objects of their IP that can be directly linked into a ConvergenSC simulation."

About the Integration

Carbon's SPEEDCompiler™ software reads synthesizable Verilog and generates a high-performance engine-DesignPlayer-that now includes an optional SystemC wrapper. DesignPlayer is a software object that can be directly linked into a SystemC simulator, such as CoWare's ConvergenSC. In contrast to co-simulation approaches, a DesignPlayer engine becomes part of a unified SystemC simulation.

DesignPlayer can represent one or more chips and multiple engines can represent a system that encompasses hundreds of millions of gates. DesignPlayer is a soft-model that is accurate to the hardware-cycle and register accurate. Unlike behavioral models or C models generated from an ideal specification, DesignPlayer behaves exactly like the hardware with all its errata. Hardware designers now have the cycles they need to run complete regression suites before chip tapeout. Software designers can finally test and debug their code on a high performance, cycle accurate, linkable model. Customers get an executable specification that contains the silicon errata for system integration and test.

About Carbon Design Systems

Carbon is delivering software products that enable high-performance pre-silicon chip and system validation. Carbon's single engine solution-DesignPlayer-can be used for hardware, software, and customer design validation. The DesignPlayer engine boosts hardware regression performance and validates drivers, diagnostics, & firmware up to 50X faster with cycle and register accuracy. A low-cost executable or linkable model can be deployed across the enterprise and to customers without the encumbrances of a slow simulator.

Carbon's new approach shortens schedules and accelerates time-to-profit by enabling validation to occur in parallel with hardware development. Product schedules can be cut significantly, with validation starting as early as the first stable RTL. Problems are found and resolved before fabrication-rather than waiting for custom models to be built or silicon to be delivered.

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